CIRCUIT OPTIMIZATION FOR MINIMUM PATH TIMING VIOLATIONS

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ABSTRACT

A method is provided to optimize delay insertions for reducing timing violations. The method includes inserting a buffer between a driver and a receiver in a timing path and placing the buffer either inside or outside a bounding box that encloses the driver and the receiver. The placement of the buffer inside or outside the bounding box creates the appropriate effective loading on the buffer to generates the required minimum delay to avoid timing violations.